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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,672	08/16/2006	Hugues Lefevre	4004-070-30 NATL	4087

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EXAMINER	
GREEN, TELLY D	
ART UNIT	**PAPER NUMBER**
2822	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/541,672	LEFEVRE, HUGUES	
	Examiner	Art Unit	
	Telly D. Green	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/16/2006*. (6-16-06)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **12-14, 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Day **(WO 2004/009349)** in view of Giron et al. **(US Patent Application 2004/0053125 A1)**.

In regards to claim 12, Day discloses two glass sheets **(Fig. 1, items 5 and 6)** and one or more thermoplastic (polyvinlybutyral is a known thermoplastic) interlayers **(page 6, line 24, Fig. 1, item 7)**, characterized in that light emitting diodes are inserted between the two glass sheets **(page 6, lines 21-23, Fig. 1, items 5 and 6)**, a connecting circuit **(item 3, flexible circuit board, 8 connection area)** being formed from a least one conductive layer deposited on one face of the glass sheets or of the thermoplastic interlayers **(page 6, lines 27-30, Fig.2, item 9)**, the conductive layer

being divided in at least 2 distinct areas **(page 6, lines 27-30, Fig.2, item 9)**, but fails to disclose each area being bound to an electrode.

However, Giron et al. disclose that electrodes can be in the form of two electroconductive layers on each side the layer or various active layers of a system **(paragraph 17, 80).**

Giving the teachings of Giron et al., it would have been obvious to one of ordinary skill at the time the invention to modify the laminated glazing of Day with electrodes in the form of electroconductive layers.

Doing so would provide a configuration easy to obtain being that it is possible to do deposit the conductive layer of the a desired surface.

In regards to claim 13, Day discloses the claimed invention but does not specifically disclose that the conductive layer has a thickness in the range of between 0.02 and 0.5 micro/between 0.2 and 0.4 micro. It is obvious to one having ordinary skill in the art at the time the invention was made to set a thickness in the range of between 0.02 and 0.5 micro/ between 0.2 and 0.4 micro, for the conductive layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Doing so would provide a sufficient thickness that would necessitate the use of sufficient heat and pressure to attach one or more electronic devices (LEDs).

In regards to claim 14, Day discloses the claimed invention but does not specifically disclose that the conductive layer has a resistance in the range of between 2 and 80, 10 and 80, or 12 and 20 Omega/sq.. It is obvious to one having ordinary skill in

the art at the time the invention was made to set a thickness in the range of between 0.02 and 0.5 micro/ between 0.2 and 0.4 micro, for the conductive layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Doing so would provide a sufficient range of resistance that would necessitate the use of various voltages.

In regards to claim 17, Day discloses the claimed invention except for electronic components having a thickness less than or equal to 3mm/less than or equal to 0.2 and 1.2mm. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have electronic components that have a thickness of less than or equal to 3mm /less than or equal to 0.1 and 1.2mm, since it has been held that discovering an optimum value of a result effective variable **involves** only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Doing so would provide a sufficient thickness that would the use of more electronic devices/components (LEDs).

Claims **15, 16, and 21**are rejected under 35 U.S.C. 103(a) as being unpatentable over Day **(WO 2004/009349)** in view of Giron et al. **(US Patent Application 2004/0053125 A1)** as applied claim **12** above, and further in view of Tanabe (**US Patent 6,379,999 B1)**.

In regards to claim 15, Day's inventions as modified by Giron et al. discloses all of the claimed limitations above except zones have been insulated from the rest of the layer by narrow insulating bands.

However, Tanabe discloses zones (item 12) have been insulated from the rest of the layer by narrow insulating bands **(items 19a,19c) (col. 6, lines 48-52, Fig. 7).**

Giving the teachings of Tanabe, it would have been obvious to one of ordinary skill at the time the invention to modify the laminated glazing of Day with zones that have been insulated from the rest of the layer by insulating bands.

Doing so would isolate the electronic circuit.

In regards to claim 16, Day's invention as modified Giron et al. and Tanabe discloses the claimed invention but does not specifically disclose that insulating bands having a width in the range of between 0.1 and 3mm/0.05 and 1.5mm/0.1 and 0.8mm. It is obvious to one having ordinary skill in the art at the time the invention was made to set a width in the range of between 0.1 and 3mm/0.05 and 1.5mm/0.1 and 0.8mm, for the insulating bands, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Doing so would provide the necessary width(s) to isolate the electronic circuit.

In regards to claim 21, Day's invention as modified by Giron et al. discloses all the claim limitations above except a zone of the conductive layer insulated from the rest of the conductor layer by narrow bands.

However, Tanabe discloses a zone of the conductive layer insulated from the rest of the conductor layer by narrow bands **(items 19a,19c) (col. 6, lines 48-52, Fig. 7).**

Giving the teachings of Tanabe, it would have been obvious to one of ordinary skill at the time the invention to modify the laminated glazing of Day with zones that have been insulated from the rest of the layer by narrow bands.

Doing so would provide a way to isolate the electronic circuit.

Claims **18-20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Day **(WO 2004/009349)** in view of Giron et al. **(US Patent Application 2004/0053125 A1)** as applied claim **12** above, and further in view of Arndt (**US Patent 6,376,902 B1)**.

In regards to claim 18, Day's invention as modified by Giron et al. discloses all the claim limitations above except that the LED's comprise several semiconductor chips in a casing.

However, Arndt discloses the LED's comprise several semiconductor chips in a casing **(col. 4 lines 49-52, col. 5 lines 13-18, Fig. 1B).**

Giving the teachings of Arndt, it would have been obvious to one of ordinary skill at the time the invention to modify the laminated glazing of Day with LED's comprised of chips in a casing.

Doing so would provide a thermal connection for heat conduction away from the LED and semiconductor.

In regards to claim 19, Day's invention as modified by Giron et al. and Arndt discloses the claimed invention except the casing is dimensioned such that the length and/or a width are at least 10/20/40-times larger than it's thickness. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a casing that is dimensioned such that the length and/or a width are at least 10/20/40-times larger than it's thickness, since it has been held that discovering an optimum value of a result effective variable **involves** only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Doing so would provide a case with the necessary length/width to cover or protect the electronic components/chips.

In regards to claim 20, Day's invention as modified Giron et al. and Arndt discloses the claimed invention but does not specifically disclose that the casing is dimensioned such that the length and/or a width in the range between 5 and 100mm/15 and 75mm/ 25 and 50mm. It is obvious to one having ordinary skill in the art at the time the invention was made to set a length and/or width in the range of between 5 and 100mm/15 and 75mm/ 25 and 50mm., for the casing, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable ranges involves only routine skill in the art (In re Aller, 105 USPQ 233).

Doing so would provide a case with the necessary length/width to cover or protect the electronic components/chips.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited for disclosing related

limitations of the applicant's claimed and disclosed invention.

Fanton et al. US Patent Application 2004/0100676 A1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Telly D. Green whose telephone number is 571-270-3204. The examiner can normally be reached on Monday thru Friday 7:30 AM - 5:00 PM EST..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Telly Green
October 29, 2007

Zandra V. Smith
Supervisory Patent Examiner
6 NOV. 2007